Data Sheet

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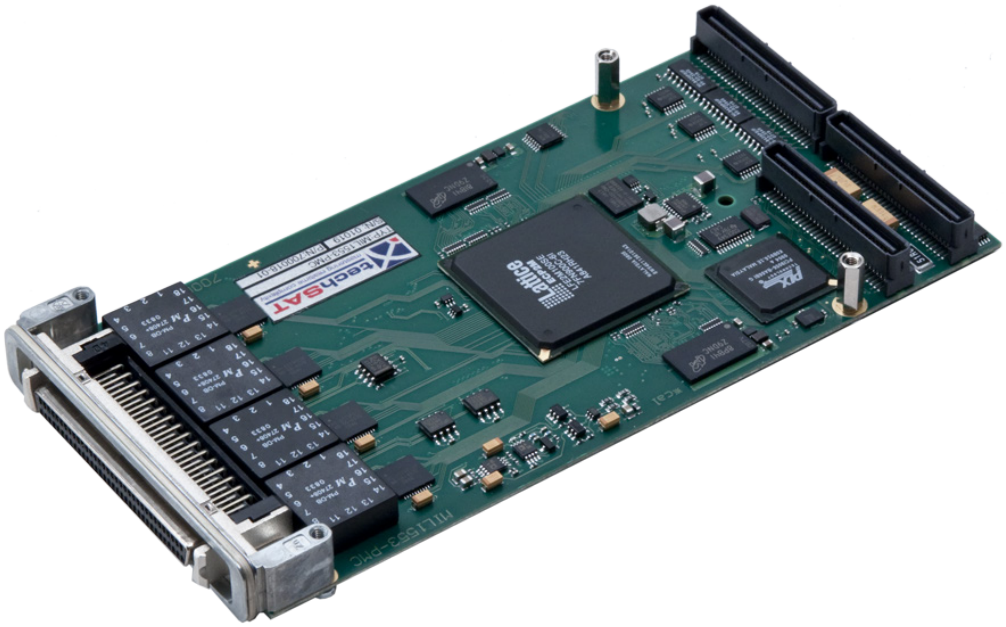
MIL1553-PMC

MIL-STD-1553B Notice 4 Compliant PMC Module



- Powerful MIL-STD-1553 interface with up to 4 dual-redundant channels
- Available as either multi-function or single-function BC, mRT, and BM
- MIDS LVT compliant
- High-performance data transfer to host using DMA block transfers
- On-board FIFO data buffering Tx and Rx
- Flexible transmit schedule definition (bus list, transaction table)
- Provides integration for PCI, cPCI, PXI, and PCIe hardware platforms
- Driver and API support for Windows and Linux

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MIL-STD-1553B Notice 4 Compliant PMC Module

Overview

The TechSAT **MIL1553-PMC** is a powerful MIL-STD-1553B notice 4 compliant interface implemented on a PMC (PCI Mezzanine Card) form factor module. The 1553 protocol is implemented in on-board FPGA logic, thus off-loading the host significantly. MIL1553-PMC is equipped with 4 dual-redundant 1553 channels. The module is available in a multi-function and in a single-function version.

Features

In addition to the 1553 protocol, MIL1553-PMC also includes comprehensive test features such as error injection/detection, triggering, and avionics discretes. One trigger IN channel is provided to start the bus controller (BC) and/or the bus monitor (BM). One trigger OUT channel is provided to notify of a receive error, start of BC, or start of a minor frame time block. Furthermore, MIL1553-PMC provides 5 bidirectional avionics discrete GND/OPEN signals.
1553 messages can be defined as either periodic or aperiodic messages. The latter can be prioritized as high or low priority. High priority messages are processed immediately. Low priority messages are transmitted after periodic messages using the remainder of the minor frame time.
All on-board clocks can be synchronized to an external time source (for example IRIG-B) allowing highly accurate receive and transmit timing.
Field firmware updates and upgrades are possible at the customer's site.

Extended Features

To ensure a high-performance data transfer between the hardware and the user application, MIL1553-PMC uses DMA block transfers directly from an on-board FIFO (Tx and Rx) buffer to the user application memory. Rx FIFOs are 8 MB per channel, Tx FIFOs 512 kB per channel.
Transmit schedule definitions are kept flexible by building schedules via references to message objects stored in the Message Object Pool. The transmit schedule is defined by either using multiple transaction tables or assigning multiple sending rates to messages (in multiples of minor frames). Each transmit schedule has an independent minor frame rate. It is possible to dynamically switch between different transaction tables or bus lists.
The BC and each individual RT simulation are accessible from independent applications. This way quite complex MIL1553 scenarios can be reproduced. Conditional bus list branching is supported. Extensive on-board HW filtering and triggering capabilities off-load applications considerably.

Software and Hardware Support

Using dedicated carriers, MIL1553-PMC provides integration for PCI, cPCI, PXI, PCIe, and VME platforms. In addition, it provides a 68-pin SCSI front connector as well as a PMC rear I/O connector.
MIL1553-PMC is shipped with a driver and API library providing the application programmers with comprehensive means to program the interface card according to their specific requirements. Drivers and APIs are available for Windows and Linux platforms.

Technical Data

General
- Compliant with MIL-STD-1553B notice 4
- 4 dual-redundant channels
- Multi-function (1 BC, 32 RT, and 1 BM) or single-function (1 BC, 32 RT, or 1 BM)

Host Interface
- PCI 2.2 Standard, 33/66 MHz, 32-bit interface
- Compatible with 3.3 V VIO and 5 V PCI VIO

Extended Features
- DMA block transfer support
- On-board FIFO data buffer, Tx and Rx
- On-board HW filtering
- Flexible transmit schedule definition
- Support of multiple transaction tables and multiple sending rates
- Internal / external trigger
- IRIG-B time synchronization
- 1 µs receive timestamp resolution
- Message callback / interrupt handling
- Optional conformal coating

Error Injection / Detection
- Bit count error
- Inverted sync error
- Mid-bit and mid-sync
- Programmable response
- Parity error
- Respond with wrong address
- Bi-phase error
- Response on wrong bus
- Word count error
- Message gap error

Additional I/O
- 5 bi-directional avionics discretes
- 1 TTL trigger IN
- 1 TTL trigger OUT

Platform Support
- Provides integration for PCI, cPCI, PXI, PCIe, and VME hardware platforms
- SDK with C API and driver available for:
  - Windows 10 64 bit
  - CentOS 5 32 bit
  - CentOS 7 64 bit
  - Drivers for other platforms on request
- LabVIEW VIs available on request

Physical Dimensions
- Single size PMC: 74 mm x 149 mm

Operating Environment
- Commercial temperature range: 0 °C to 60 °C
- Extended temperature range (on request): –20 °C to 80 °C

Part Number
- 700018

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