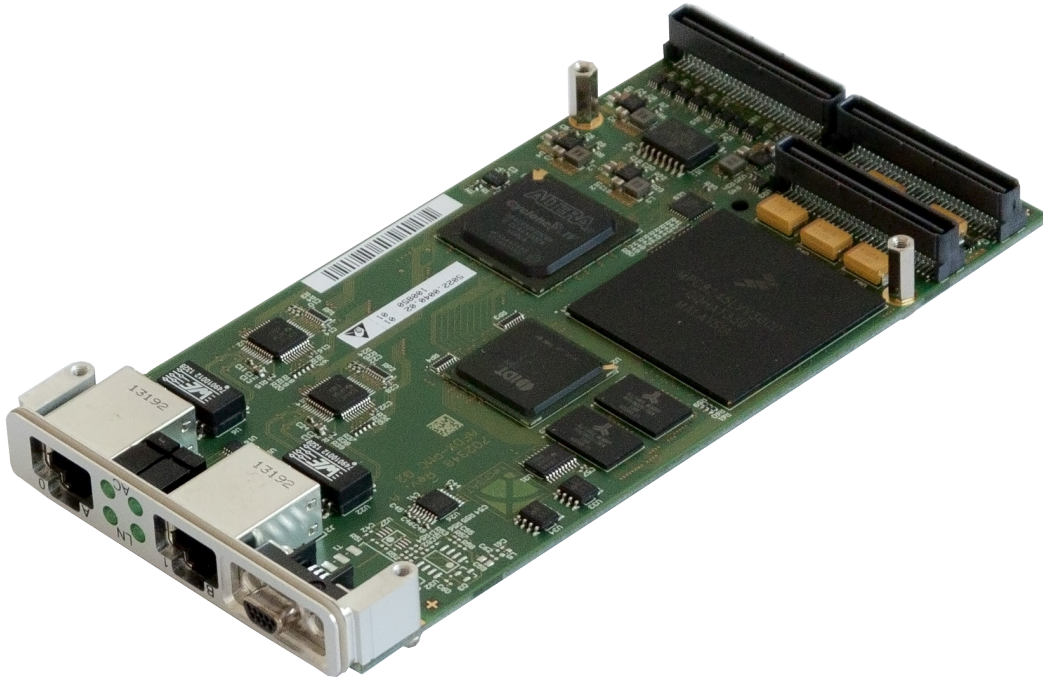


# AFDX-PMC-2G

## AFDX®/ARINC 664 PMC Module



- On-board AFDX® protocol stack implementation
- Airbus and Boeing AFDX® compliant protocol stack
- Two full duplex AFDX® networks that can be operated in either independent or dual-redundant mode
- Comprehensive error detection and filtering features
- Applicable on PCI, cPCI, PXI, and PCIe hardware platforms
- Driver and API support for Windows and Linux



# AFDX-PMC-2G

## AFDX®/ARINC 664 PMC Module

### Overview

TechSAT's **AFDX-PMC-2G** is a powerful AFDX®/ARINC 664 interface implemented on a PCI Mezzanine Card (PMC) form factor module. It implements the Airbus and Boeing AFDX® protocol stack in on-board firmware and FPGA logic, thereby offloading the host.

AFDX-PMC-2G is equipped with two full duplex AFDX® networks that can be operated in either independent or dual-redundant mode. The AFDX-PMC-2G connector is a twisted pair copper interface.

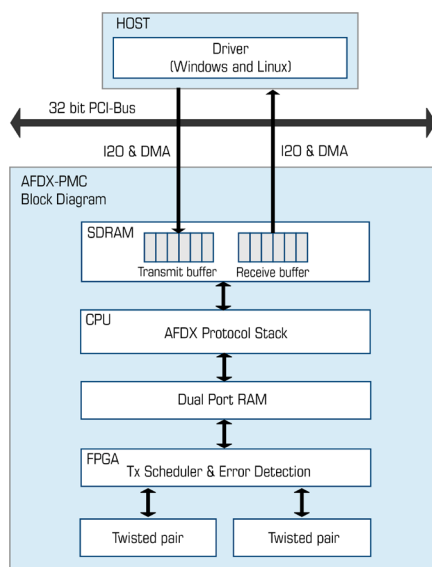
In addition to the AFDX® protocol stack, the AFDX-PMC-2G also implements comprehensive test features such as error detection and filtering. Optimized for performance, the AFDX-PMC-2G is ideal for applications such as AFDX® End System (ES) testing and validation, ES simulation, and ARINC 615A data loading via AFDX®.

### Software Support

AFDX-PMC-2G is shipped with a C API, a Python 2.6 API, and drivers for Windows and Linux. In addition, several software tools for test, simulation, and data loading purposes are available on request. For test purposes, TechSAT has developed a powerful AFDX® ES test and validation tool. Furthermore, TechSAT has developed several AFDX® based protocol simulations for the Airbus A350, A380, and A400M as well as for the Boeing 787. Finally, AFDX-PMC-2G also supports the TechSAT tool suite for data loading over ARINC 615A.

### Architecture

As depicted in the block diagram, the host communicates with the AFDX-PMC-2G via a dedicated driver. The driver uses I2O and DMA for fast data transfers between the host and the AFDX-PMC-2G. The on-board CPU runs the AFDX® protocol stack and controls the FPGA, which offloads the CPU by handling Tx scheduling and error detection.



### Technical Data

#### General

- Applicable on PCI, cPCI, PXI, and PCIe platforms
- 32 bit @ 33/66 MHz PCI-bus interface
- Compliant with Airbus and Boeing AFDX® protocol
- Optional support for EDE protocol (only Boeing compliant AFDX® protocol)
- Time synchronization to TechSAT Timemaster
- Twisted pair transceivers
- Auto-negotiation or fixed 10/100 Mbps transmit rate
- 10/100 Mbps receive rate
- Down to 500 µs BAG configuration
- Command FIFOs

#### Transmission & Reception

- Traffic shaping via VL and BAG configuration
- Integrity checking and redundancy management
- Up to 253 transmit VLs
- Up to 1024 ports per VL
- Up to 510 receive VLs
- Virtual Links (VL) and Sub-VL
- 1 µs Rx frame timestamp resolution
- Transmit and receive statistics
- UDP and IP protocol including IP fragmentation and re-assembly
- AFDX addressing with multicast or unicast addresses
- Sampling and queuing ports for transmit and receive
- Autonomously scheduled transmissions
- TAP capable

#### Error Detection

- CRC, IFG, short preamble, and nibble errors
- RSN detection enabled/disabled
- Wrong Ethernet type

#### Software

- SDK with C API, Python 2.6 API, and drivers available for the following platforms:
  - Windows® 10 64 bit only
  - CentOS 5 32 bit
  - CentOS 6 32 bit/64 bit
  - CentOS 7 64 bit only
  - Drivers for other platforms on request
- LabVIEW VIs available on request
- Optional software tools for test, simulation, and data loading

#### Physical Dimensions

- Size: 74 mm x 149 mm x 13.5 mm

#### Operating Environment

- Operating temperature: 0 °C to 55 °C
- Storage temperature: -40 °C to 70 °C
- Humidity: 5% to 90% non-condensing

#### Power Consumption

- max. 7.5 W

#### Part Number

- 702348-02

AFDX® is a registered trademark of Airbus